

FINE PITCH CU PILLAR ASSEMBLY CHALLENGES FOR ADVANCED FLIP CHIP PACKAGE

Nokibul Islam, Ming-Che Hsieh*, Kang KeonTaek**, Vinayak Pandey

STATS ChipPAC, Inc.

*STATS ChipPAC Pte. Ltd.

**STATS ChipPAC Korea

nokibul.islam@statschippac.com

However, there is a high risk for cracking or delamination of the very fragile extremely low-k (ELK) layer or the advanced Si node anTwb[(au[(a(ela)p[(an)412(t)-3()-2(cr)-5(ac)-)-4k)6(in)(Twc)-3(in)(Twt14(m))6(ien)4122a(ela)frau618()-2(c15(tu-3(h

in the process. Figure 4 shows a typical cross-section picture of bumps for various interconnection technologies. No significant warpage, bump tearing, non-wet, or bump alignment was observed in the LAB process. In the TCNCP process,

Figure 9: Package warpage with temperature for 60um bump pitch, MRP process

Figure 10: Fine pitch fcFBGA long term reliability data with MRP process

To prove LAB technology for fine pitch Cu pillar applications, a few other test vehicles (TV) were built to collect more CPI data, process margin and comprehensive reliability. One of the examples was a fcFBGA package with 13X13mm body size, 8X9mm die size with 16FF silicon and 85um Cu pillar bump pitch with one trace between the bumps. Similar to the previous 60um bump pitch program QTC, CSAM, warpage and JEDEC standard full package reliability were also performed as shown in Table 3 and bump cross-section pictures are in Figure 11 below. There was no anomaly in the bump structure and the joints are perfectly aligned.

Table 3: Fine pitch fcFBGA long term reliability data with LAB process

Figure 11: Fine pitch Cu pillar bump cross-section data after standard reliability tests

Fine Pitch Cu Pillar in fcBGA

Fine pitch Cu pillar bump has experienced growing adoption in high performance and low-cost area array flip chip BGA (fcBGA) packages as well. In area array bumps, assembly challenges are much more prevalent than typical perimeter array fcFBGA packages. Similar to perimeter array fcFBGA bumps, TCNCP is one of the alternative solutions for fine pitch bumps in fcBGA. However, the cost, bump misalignment and ELK crack are still major concerns here. In this study LAB technology was also investigated for several area array fine pitch bump fcBGA packages. Very similar results were found in fcBGA packages. For a 17X17mm fcBGA with a heat spreader (fcBGA-H) and 4 MCM dies that were each 7X5mm in size and 60um UBM, a 180um Cu pillar bump was used in the TV. A relatively thicker die (350um) was used for the TV. Both MR and LAB processes were used in the study. The temperature profile for LAB at various locations on the packages were measured and plotted as shown in Figure 12. The maximum temperature location was in the die while the minimum was in the substrate. There was no significant temperature gradient observed in the substrate. Total reflow time was a little over 1 sec.

A small number of units from each leg (MR and LAB) were selected for destructive failure analysis (FA) and intermetallic morphology analysis. The IMC growth mechanism in this study is illustrated in Figure 13. At reflow stage, Ni-Sn IMC was formed at the interface between the Ni layer and solder, and Cu-Sn IMCs were formed at the bonding interface between Cu pad and solder. In comparing the two pictures, it is somewhat clear that less IMC formed with LAB process as compared to MR due to longer thermal exposure of MR during the attach process. More investigation will be required to verify it.

Figure 13: IMCs growth behaviors between the two processes

CONCLUSION

With the phenomenal expansion of various fine pitch Cu pillar attach technology offerings and manufacturing footprints, assembly suppliers are positioning themselves to support the strategic need for very cost effective, high performance packages for various fine pitch applications. With the evolution of different new flip chip attach technologies, it is expected that significant cost can be associated with the new technology to overcome assembly related yields. Standard MR to latest LAB attach technologies were described in the paper.

Several case studies with fine pitch Cu pillar bumps were considered in this study. The QTC test with temperature range of -40 C to 60 C along with JEDEC standard reliability tests were performed to confirm if there was any white bump phenomenon in the CPI work or any other long term reliability related failures. Invariably, all the cases found that MR has minimal limitations for very fine pitch Cu pillar assembly process. LAB is a new technology that can potentially be used as an alternative to MR for very fine pitch applications. However, the industry is will continue to extend the MR process window to make a robust and cost effective solution for fine pitch flip chip. From the literature, a conclusion can be reached that MR has the highest throughput as compared to LAB or TCNCP. Typically, TCNCP is about one quarter to one third of MR and LAB is about half to three fourth for MR. More investigation and further study is needed to support the above statement.

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REFERENCES

- [1]. S. Movva, S. Bezuk, O. Bchir, M. Shah, M. Joshi, R. Pendse, -Column on BOL) technology: A low cost flip chip solution scalable to high I/O density, fine bump pitch and advanced Si-Conference (ECTC), pp. 601-607, 2011.
- [2]. Ming-Che Hsieh, Chi-Yuan Chen, Ian Hsu, Stanley Lin